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Efficient optimization of fully-integrated inductive DC-DC converters comprising tapered inductor layout synthesis and temperature effects

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Abstract The evolution of computer-aided design tools has extended the capabilities of a designer by pushing the optimality of complex circuits beyond the ad hoc manual implementation. This work presents a framework to co-optimize the circuit and the layout parameters of fully integrated inductive DC-DC converters. The framework comprises expensive optimization that is speeded up by active learning sample selection and evolutionary techniques to acquire an optimal converter. A tapered inductor topology is used to increase the quality of the on-chip inductor and to improve the efficiency of the overall monolithic DC-DC converter. The optimization framework is validated by co-optimizing the design parameters and the tapered inductor layout for a fully-integrated DC-DC boost converter in a $0.13\mu m$ CMOS technology. The power loss in the circuit is reduced with 27 % resulting in a 7 % efficiency improvement, compared to a fully-integrated DC-DC boost converter with a regular inductor topology.

Keywords DC-DC converters · Expensive optimization · Active learning sample selection · Layout-based modeling · Tapered inductor layout

1 Introduction

It becomes more cost-efficient to integrate power management circuitry on the same die [1]. An example of such a circuit is a DC-DC converter. This also implies that all the passives must be integrated on-chip in these DC-DC converters. To achieve higher performance and efficiency, the design of these passives is paramount for the overall performance of the monolithic solution.

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Design tools can be used to explore and optimize in this design space, to achieve this higher efficiency. Many interesting techniques are emerging in the domain of artificial intelligence (AI) that can simplify the work of an analog circuit designer. Up to now, the task of this designer was rooted on years of design experience and thorough circuit knowledge. The envisaged AI techniques target the reduction of the simulation and design time, the optimization of the entire circuit topology and its design parameters [2] as well as the layout synthesis of the integrated passive components [3]. Moreover, inexperienced designers are now able to identify circuit trade-offs more efficiently, while more experienced designers can boost the optimality of their designs even further.

In this work, a layout-aware optimization framework has been developed and used in order to optimize the complex trade-offs in DC-DC converter circuits. The optimization framework entails evolutionary methods for the optimization of the design parameters on different abstraction views of the design, starting from a high-level system description using differential algebraic equations (DAE) in Matlab and ending up with a synthesized layout of key components. The expensive evaluation of each synthesized layout candidate is efficiently optimized by active learning sample selection. A schematic overview of the optimization framework is shown in Fig. 1. The design is optimized across different layers of abstraction.

In order to achieve a high accuracy, the DC-DC converter is modeled at each abstraction layer and the corresponding optimization is done. The effect of the inductor topology and temperature effects are taken into account in the lowest (physical) abstraction layer. Moreover, this paper presents a tapered on-chip inductor topology that enables an efficiency increase compared to regular inductor topologies. No added

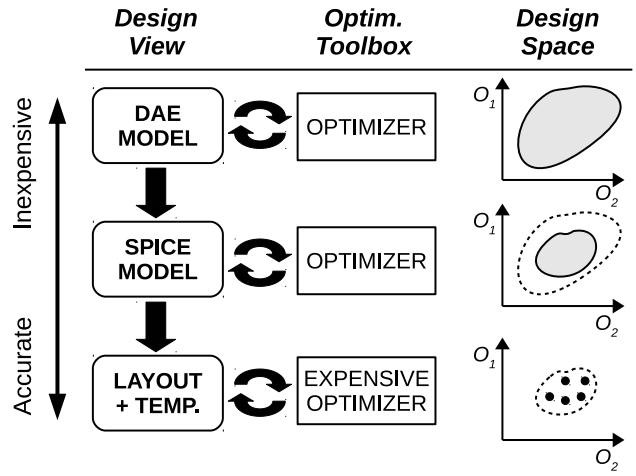

Fig. 1 Overview of the framework: The design is implemented in different layers of abstraction (design view) and appropriately optimized in each layer. The design space is refined as the level of implementation increases.

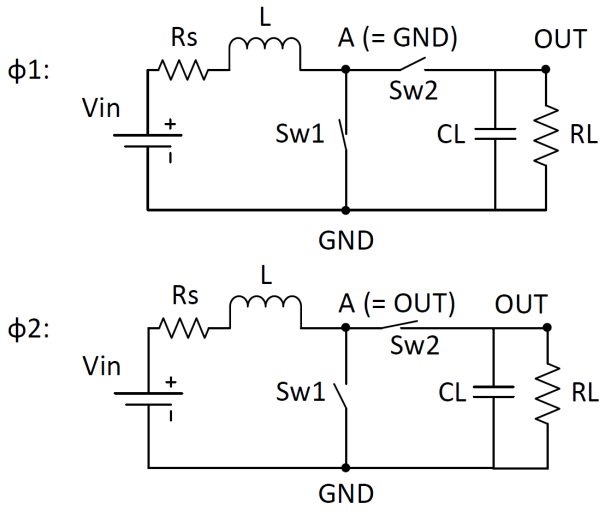

Fig. 2 Basic DC-DC converter circuit, two phases depicted.

cost is introduced in the processing steps.

The paper is organized as follows. In section 2 the architecture of the inductive DC-DC converter is discussed along with the modeling. Section 3 introduces the tapered inductor topology. In section 4 the optimization framework is developed. Section 5 gives an overview of the experimental results and conclusions are drawn in section 6.

2 Architecture of the DC-DC converter

2.1 Inductive DC-DC boost converter

A basic circuit of an inductive DC-DC boost converter is depicted in Fig. 2. The circuit operates in two phases. During the first phase, as shown in the top part of Fig. 2, the inductor is charged and the output capacitor is discharged. During the second phase, there is a transfer of energy from the inductor towards the capacitor. In this way, the capacitor is charged again, and the output voltage rises. Based on the timing of these two phases, the output voltage is determined. It is to be noticed that the voltage U_A at the output of the inductor (node A) switches between GND and OUT. This will be of importance in section 3.

For more than 50%, the efficiency of the converter is determined by the power loss in the inductor [11]. Hence, the quality factor of the inductor is of paramount importance. All power to the load needs to be delivered through the inductor. This implies that the series resistance of the inductor determines the efficiency of the complete circuit. Furthermore, the parasitic capacitive coupling of the inductor to the substrate leads to power losses.
Different approaches exist to increase the quality factor of inductors. One way to achieve this is to apply ferro-magnetic materials to the metal-track inductors [12] or by using bond-wire inductors [13]. Another way is the addition of a thick metal-film on top of the chip [14], under-etching of the substrate [15], or even the use of an aluminum substrate [16]. However, these are expensive methods. In the tapered inductor topology, presented in section 3, the standard CMOS process is used without the need for additional costly processing steps.

2.2 High-level circuit model

A high-level circuit model has been designed for this DC-DC boost converter in [4]. The model was designed starting from a time-domain description of the two phases in an inductive DC-DC boost converter. The resulting differential algebraic equations are merged and solved for a specific boost converter. This model enables a designer to perform an accurate evaluation (within 3% accuracy range from SPICE simulations) of the converter performance, using specified circuit parameters. No time-intensive SPICE simulations of the full circuit are therefore needed anymore. The model, as was designed in [4], takes into account the resistive and dynamic losses in the converter circuit and is implemented as a system of differential algebraic equations. Several design variables for this model are indicated in Table 1. The reader is referred to [4] for a more in-depth discussion of the derivation of the differential algebraic equations, this is out of the scope of this paper.

The original model has been enhanced by the authors to include layout-aware modeling and temperature effects. The layout-aware modeling will be discussed in section 3; the temperature effects are discussed in the following section.

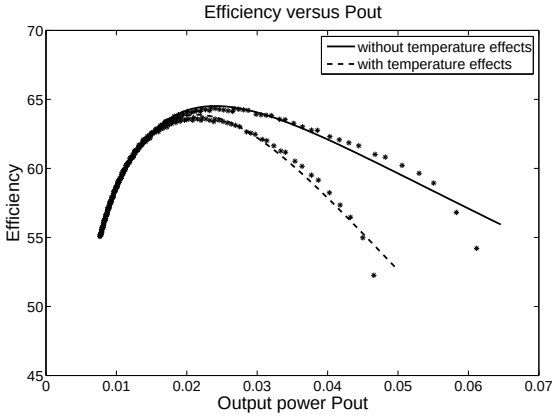

Fig. 3 Temperature effect on the converter efficiency for varying output power.

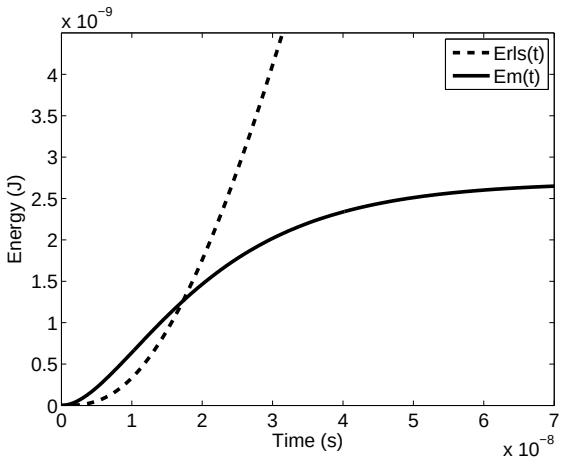

Fig. 4 Stored energy $E_m(t)$ in the inductor and lost energy $E_{Rls}(t)$ in the parasitic series resistance as a function of the charging time.

2.3 Temperature effects

The efficiency of a converter can never be 100%. Indeed, power losses are always present in the (parasitic) series resistances. The effect of these power losses is an increased temperature on-chip. This increase will have effects on the circuit: the on-resistance of the switches and the series resistance of the inductor will rise. One can determine a decreasing efficiency for an increasing output power. This trend was measured in [17]. The existing model of [4] has been enhanced by the authors of this paper to incorporate these effects. Fig. 3 indicates the difference between the basic model without temperature effects and the enhanced model with temperature effects incorporated.

2.3.1 Causes for efficiency decrease

Two things need to be explained. On the one hand, a global efficiency decrease is present. On the other hand, an extra efficiency decrease due to the increasing temperature is present.

Global efficiency decrease:
The cause for the global efficiency decrease can be found through the inductor. The magnetic energy that is stored during the first phase will increase with time and saturate. There will be dissipated energy in the series resistance of the inductor as well, increasing with time. At high output power, the duty factor is higher, meaning that the inductor is charged for a longer time and the energy loss in the parasitic series resistor will be higher as well. This is depicted in Fig. 4: $E_m(t)$ (the stored magnetic energy in the inductor) and $E_{Rls}(t)$ (the dissipated energy in the parasitic series resistance) are plotted. After some time, the energy will mainly be lost in the series resistance without extra energy being stored in the inductor. Therefore, the efficiency of a DC-DC converter decreases with higher output power, as can be seen in Fig. 3.

Efficiency decrease due to temperature increase:
Apart from the global efficiency decrease, a decrease in efficiency is present at increasing temperatures. At higher output power, more power losses exist in the parasitic resistances. This implies that the on-chip temperature will increase. The most important effect of this is the increase in on-resistance of the switches. Because of the extra heat, the electrons in the channel will encounter more resistance since the Si-atoms are vibrating heavier. The current flowing through the transistor channel will decrease.

2.3.2 Simulation of on-resistance

Temperature has a large effect on the conduction losses [18]. The carrier mobility in the channel decreases with an increase in temperature. The mobility μ depends on the temperature T as follows [18]:

$$\mu(T) = \mu(T_{nom}) \left(\frac{T_{nom}}{T} \right)^m \tag{1}$$

$\mu(T_{nom})$ is the mobility measured at nominal temperature T_{nom}, m is a positive constant. With increasing temperature, the mobility decreases. Therefore, the drain current I_D in the saturation region decreases according to the following basic equation with oxide capacitance C_{OX}, gate voltage V_{GS} and treshold voltage V_{TH}:

$$I_D(T) = \mu(T) C_{OX} (V_{GS} - V_{TH})^2 \tag{2}$$

The ideal formula for the on-resistance in the linear region is given by:

$$R_{DS(on)} = \frac{1}{\mu C_{OX} \frac{W}{L}} (V_{GS} - V_{TH} - V_{DS}) \tag{3}$$

with V_{DS} the drain-source voltage, W and L the transistor width and length. The on-resistance as a function of the temperature can then be expressed as:

$$R_{DS(on)}(T) = R_{DS(on)}(T_{nom}) \left(1 + \frac{\alpha}{100}\right)^{T-T_{nom}} \quad (4)$$

In this equation, α is the temperature coefficient. From this equation, one can see that the on-resistance $R_{DS(on)}$ increases with increasing temperature T.

The effect of this increasing on-resistance can of course be checked in a SPICE simulation. However, it is interesting to be able to explore the temperature effects in the high-level model without requiring time-consuming SPICE simulations. Equation (4) gives a good estimation for the value of $R_{DS(on)}$ already. To make the extended high-level model even more accurate, a look-up table has been made. The input parameters to the table are the temperature and the transistor sizes. The look-up table is then created by a series of SPICE simulations for transistors at discrete points of varying temperature and transistor sizes. This is a one-time effort. Based on these results, a fitting is made for the output resistance as a function of the transistor width and temperature.

$$R_{DS(on)}(W,T) = p_1(W,T).V_{DS}^3 + p_2(W,T).V_{DS}^2 + p_3(W,T).V_{DS} + p_4(W,T) \quad (5)$$

In the look-up table, the fitted coefficients $p_i(W,T)$ are saved, associated with a discrete width W and temperature T. Based on these coefficients, every point in between can be calculated using the interpolation. The differences between the fitted results using the look-up table and equation (4) are given in Fig. 5. Both of these are compared with a SPICE simulation. It can be seen that the look-up table approaches the SPICE results accurately. On average, the mismatch between the fitted model (using the look-up table) and SPICE is only 1%, while the error for equation (4) can even be around 30%. From Fig. 5 it can be determined that equation (4) is only a rough estimate. It is thus appropriate to use the look-up table to achieve better high-level modeling.

2.3.3 Series resistance of the inductor

Because of the on-chip heating, the series resistance of the inductor will increase as well. This implies higher power losses in the inductor. A simple formula can be used to calculate the series resistance of the inductor:

$$R_{Ls,temp} = R_{Ls} * (1 + \beta * \Delta T) \quad (6)$$

In this equation, R_{Ls} is the inital series resistance at a reference temperature of $25°C$. ΔT is the temperature rise and β is the temperature coefficient of the resistivity of the metal tracks.

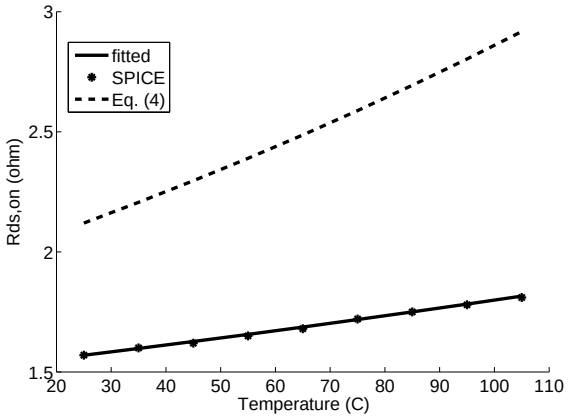

Fig. 5 On-resistance vs. temperature. Simulation results for the simple formula (4), SPICE and the fitted result (5) using a look-up table.

2.4 SPICE circuit model

For modeling at the circuit level, a SPICE circuit model has been designed for the simulation of the DC-DC converter topology. This model is closely related to the basic model depicted in Figure 2, but takes the extra parasitics into account that will be present in a realistic situation. The switches are now modeled using the BSIM model, starting from a given width W and length L. This enables a more accurate simulation of the complete converter. In contrast to the high-level DAE model where the operation of the switches was linearized, the BSIM model takes into account all transistor effects present, yielding a more accurate estimation of the behaviour of the switches. However, due to the introduced parasitics in the SPICE model, several time-constants are introduced in the circuit and these will increase the total simulation time.

2.5 Finite element model

For modeling at the physical level, accurate field- and electromagnetic (EM) solvers are needed to estimate the parasitics that are present in the layout, given a set of design variables (cf. Table 1). These parasitics include, for instance, the parasitic substrate capacitance and series resistance of the inductor, as will be discussed in section 3. However, these type of simulations increase the simulation time even more, compared to the SPICE circuit model. This efficiency problem will be handled in the optimization framework presented in section 4. In this work, the method of moments was used, applied via the FastHenry tool [8].

3 Tapered inductor topology

To achieve a high quality factor for the inductor, two aspects need to be considered. First of all, the parasitic series resis-

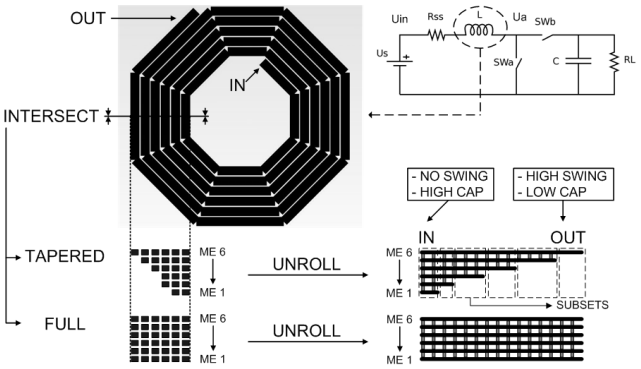

Fig. 6 Intersection of an inductor with added tapered vs. full metal layers.

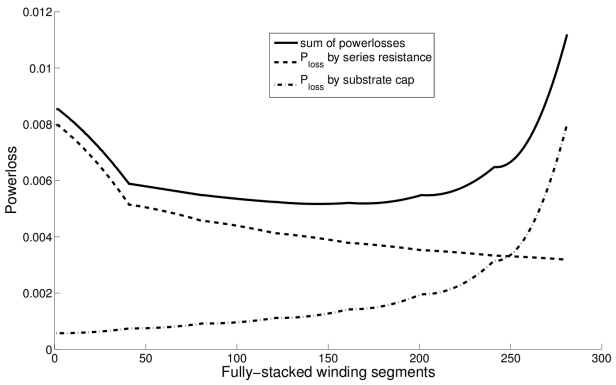

Fig. 7 Trade-off between power losses caused by series resistance vs. substrate capacitance. Number of segments indicates more added metal in layers.

tance must be as low as possible. Secondly, the inductance must be as high as possible. This is derived from the standard expression for the quality factor:

$$Q = \frac{\omega.L}{R} \tag{7}$$

The total inductance can be increased by increasing the number of windings in the inductor. However, the total length of the metal track now increases, meaning that the total parasitic series resistance R_S rises, as shown in equation (8). In (8), ρ and l denote the resistivity and length of the metal track respectively. A indicates the cross-section area of this metal track. Because of the increased length of the metal track, the total inductor area increases as well. This implies that the parasitic substrate capacitance C_{sub} (9) increases as well. In (9), ε_0 and ε_r indicate the absolute and relative permittivities of the oxide between the metal track and the substrate, A_{ovl} indicates the overlapping area of metal track and substrate, and d indicates the distance between the inductor metal track and the substrate.

$$R_S = \frac{\rho * l}{A} \tag{8}$$

$$C_{sub} = \frac{\varepsilon_0 * \varepsilon_r * A_{ovl}}{d} \tag{9}$$

The parasitic series resistance can be decreased by adding more parallel-connected metal layers. This is depicted in the *full* intersection in Fig. 6. However, since more metal layers are added, the distance of the lowest metal layer to the substrate decreases. According to equation (9), the total parasitic substrate capacitance C_{sub} now increases. Hence, the power losses in the substrate increase. This is indicated in (10), with input voltage U_S, average voltage drop ΔU over the inductor and switching frequency f_{SW}.

$$P_{loss,substrate} = C_{sub} * U_S * \Delta U * f_{sw} \tag{10}$$

A tapered inductor topology is introduced to solve this problem. In this topology, an evenly increasing number of metal layers is used for the inductor metal tracks. The number increases along the length of the metal track, going from OUT to IN. This is indicated in the *tapered* cross-section presented in Fig. 6. Compared to a solution with added *full* metal, this leads to an increase of series resistance. However, C_{sub} and the corresponding power losses are lower, because less metal is close to the substrate. A trade-off can now be determined between the series resistance and the parasitic substrate capacitance, because of the continuous distribution of the metal layers. This trade-off is presented in Fig. 7. The horizontal axis presents an increasing number of windings using a full stack of metal layers, leading to a more *full* inductor topology. The losses in the series resistance decrease while the losses in the substrate capacitance increase. The most optimal design point for an inductor can be located using this trade-off curve. This method has been incorporated into the optimization framework.

The unrolled versions of both inductors with *full* metal layers and with *tapered* metal layers are also depicted in Fig. 6, next to the intersections of the two inductor types. The tapered inductor has a decreasing number of windings with full metal stack, meaning that there are less metal layers close to the substrate. The electrical equivalent lumped model is given in Fig. 8. The subsets of this lumped model are shown in Fig. 6 for the unrolled tapered inductor. The total power loss in the substrate can now be calculated as in [4], using (11). Here, $U_{C,max}$ is the average ΔU over all subsets and $C_{sub,i}$ is the specific substrate capacitance of each subset. Using the factor $\frac{i}{n-1}$ the average total voltage drop is translated into one that is applicable for a specific subset i of the n subsets.

$$P_{loss,substrate} = f_{sw} * U_S * \sum_{i=0}^{n-1} \left(i * \frac{U_{C,max} * C_{sub,i}}{n-1} \right) \tag{11}$$

The voltage over the inductor changes frequently in a boost converter topology. The voltage U_A at node A, as seen in Fig. 2, will change from GND to OUT (large ΔU), whereas the side of the inductor at node IN is at DC voltage ($\Delta U = 0$). The substrate capacitance at the IN-side of the inductor thus

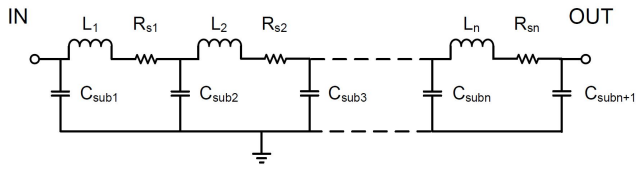

Fig. 8 The lumped inductor model.

Table 1 Design variables, simulation model and design objectives of the DC-DC converter at each layer of abstraction.

design variables	simulation model	objectives
$f_{SW}, \delta, \frac{W}{L}, R_{SW}, L, R_{load}, C_{load}$	differential algebraic equations (DAE)	$\eta, \Delta V_{out}$
W, L	BSIM, SPICE	$\eta, \Delta V_{out}$
# of layers, width, # of turns, load-dependent temperature variations	fast field solver, look-up tables, finite element solver	$\eta, \Delta V_{out}$

causes no significant power losses according to (10). At the *A*-side of the inductor, the number of metal layers is reduced yielding a lower substrate capacitance of this subset and thus lower power losses.
By introducing this tapered topology, an extra design parameter is introduced: the *tapering factor*. This factor indicates the slope of the tapered structure and determines where the inductor is on the trade-off curve of Fig. 7.

4 Optimization framework

The design variables, simulation models and design objectives are listed in Table 1 for each layer of abstraction. The layout-aware optimization of the DC-DC converter would require to synthesize the layout of the inductor for the accurate estimation of the parasitic losses, each time a candidate design is proposed by the optimizer. From this synthesized layout, an electrical equivalent circuit can be extracted either by a lumped model or by a frequency-dependent S-parameter block. However, the layout generation and evaluation is a computationally expensive task, meaning that only a small portion of the design space can be explored within reasonable CPU time. Therefore, the layered-abstraction approach of Fig. 1 is proposed to efficiently find a feasible space where all objectives and specifications are met. The relative computational complexity and the amount of possible evaluations within a fixed computation time are illustrated in Fig. 9 for each of the three abstraction layer views. Note that the (1x) in the Figure indicates the one-time effort for the layout synthesis. Once this is generated it is stored in a database.

The proposed optimization framework, depicted in Fig. 10, targets an efficient exploration of the design space by incrementally adding complexity to the simulation models. In each layer a multi-objective optimization algorithm is used. The optimization objectives are the efficiency and the ripple

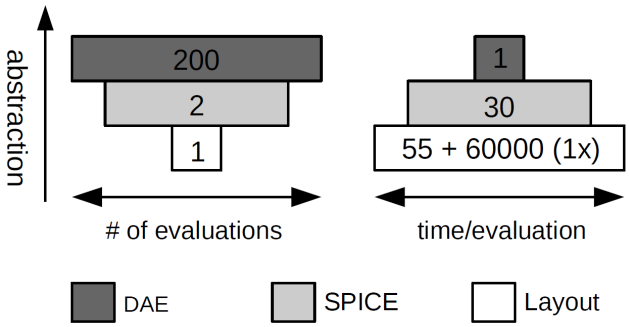

Fig. 9 Amount of evaluations within a fixed CPU time and the computational complexity at each abstraction level. Computationally cheap high-level evaluations allow a broad design space exploration.

on the output voltage, corresponding Table 1. The implementation is summarized as follows: firstly, initial samples are generated for the high-level DAE model, thereby tuning the corresponding design variables of Table 1 to their optimal value. The low evaluation cost of the DAE model allows one to explore a large amount of candidate designs. The resulting Pareto-optimal DAE designs then serve as initial seeds for further, more accurate optimization.

Next, the optimal DAE designs that have been found to be within specifications are replaced by a SPICE netlist for more accurate estimation of the switching losses. The cost of a single SPICE evaluation is high compared to the high-level DAE model due to the incorporation of the BSIM models and the execution of a transient SPICE simulation with different time constants. As a result of the optimization at this abstraction level, optimal widths and lengths for the switches are obtained.

Finally, the layout of the tapered inductor is synthesized from the approximate lumped model of section 3 for different layout parameters. The design space of the inductor layout is bounded by the optimal inductance, as calculated previously by the DAE- and SPICE-level model. Because layout synthesis is a computationally intensive task, the evaluation of this model inside an unsupervised optimization loop tends to be too costly for practical purpose. This problem is tackled by adapting an active learning sample selection strategy (ALSS) to avoid unnecessary expensive evaluations. The following sections describe each optimization step in more detail.

4.1 Unsupervised Optimization

As stated above, the coarse DAE- and SPICE-level models enable us to explore a large portion of the feasible design space. The ability to explore the design space makes up for the loss in simulation accuracy. This coarse optimization is not subjected to expensive simulation times, allowing unsupervised optimization techniques to be applied.

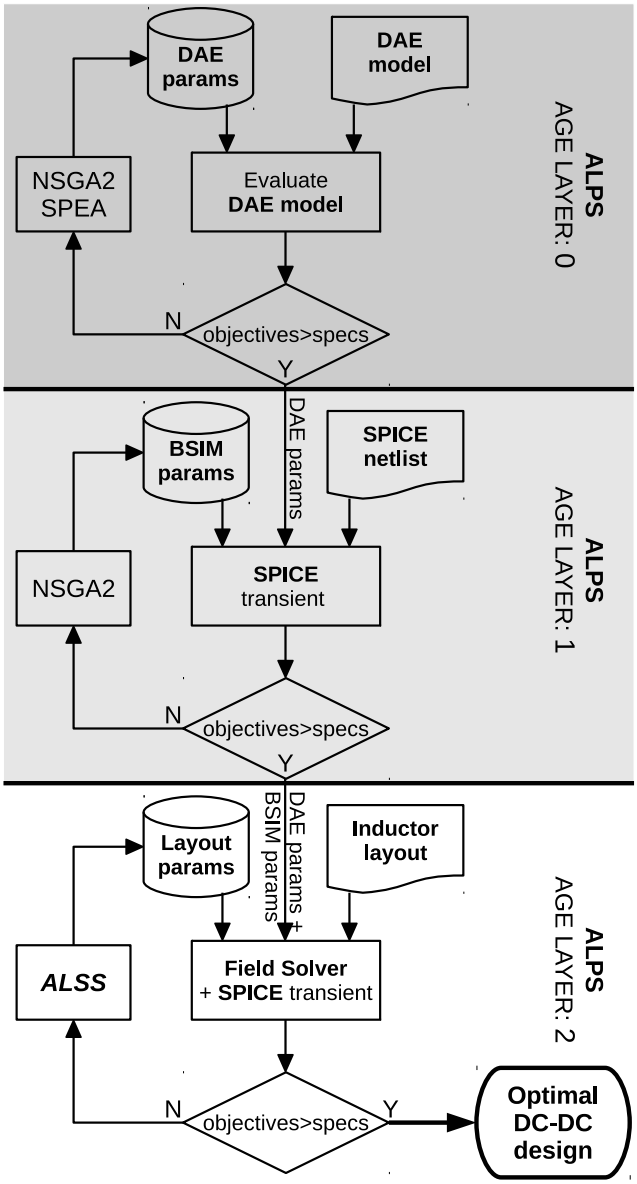

Fig. 10 Flow chart of the layout-aware optimization algorithm. Each ALPS layer adds complexity to the model and refines the design space. The optimized design parameters of each layer are passed on to the next one. The final layer comprises computationally expensive layout synthesis and is therefore equipped with an active learning sample selection algorithm for efficient optimization.

The unsupervised multi-objective optimization framework used in this work is composed of a combination of existing evolutionary techniques, e.g. NSGA-II [5], SPEA [6] and ALPS [7]. This combination yields an efficient and robust framework for the optimization of a relatively large class of analog building blocks. The ALPS platform maps directly onto the design views in Fig. 9 and Table 1. A group of age layers, as used in ALPS, corresponds to a design view.

4.2 Active Learning Sample Selection

There are two simulation possibilities for the inductor layout. The first one is to perform a fast evaluation using field solvers. An example of such a tool for the simulation of inductors is FastHenry [8]. On the other hand, when electromagnetic coupling effects need to be included, expensive evaluations are needed. For instance, finite-element solvers can generate accurate simulation results for 3D on-chip structures. In general, the expensive evaluations are more accurate than the fast lumped model evaluations.

Fig. 11 demonstrates the effect of dense and sparse sampling in the context of optimization. Undersampling leads to large regions of uncertainty in between the points, thereby impeding the search for a global optimum. This problem worsens as the number of design variables increases due to the *curse of dimensionality* [27]. One can ensure convergence to a global optimum by taking a sufficient number of samples such that the design space coverage is large. However, when dealing with expensive EM simulations, this approach becomes infeasible.

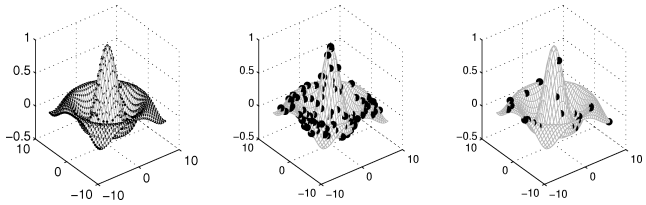

Fig. 11 Sampling of a *sinc* test function, from left to right becoming more sparse.

The total cost of the expensive simulations can be reduced using an active learning sampling selection (ALSS) technique. The available efficient computer-aided design optimization methodologies for integrated passive components can roughly be classified into 3 categories:

1. The optimization of a coarse model that can be evaluated efficiently [19]. The coarse model is typically implemented as an equivalent or lumped circuit model which is evaluated inside the optimization loop. The coarse model is implemented in the lower ALPS layers using the DAE and SPICE model, as discussed above.
2. The optimization of a local surrogate model [20]. Surrogate modeling is an engineering method used when an outcome of interest cannot easily be measured or simulated, so an approximate model is used that is computationally cheap. The local model is computed once using layout simulations around the optimum that was determined in the coarse model. Once the model exists, it is optimized *without further updating* of the model with new training points [9].

3. The generation of a surrogate model that is locally optimized combines the computational advantage of the surrogate model evaluation with the accuracy of field solvers [21], [22], [23]. After obtaining the coarse model from the lower ALPS layers, a local surrogate model is constructed by selecting base points in the vicinity of the optimum of the coarse model to train the surrogate model. Finally, the surrogate model is verified and *iteratively updated* using high-fidelity EM simulations of new design solutions in the local vicinity of the optima. The schematical flow for this active learning optimization strategy is given in Fig. 12. This approach is used in the upper ALPS layer that contains the most mature design candidates for layout synthesis.

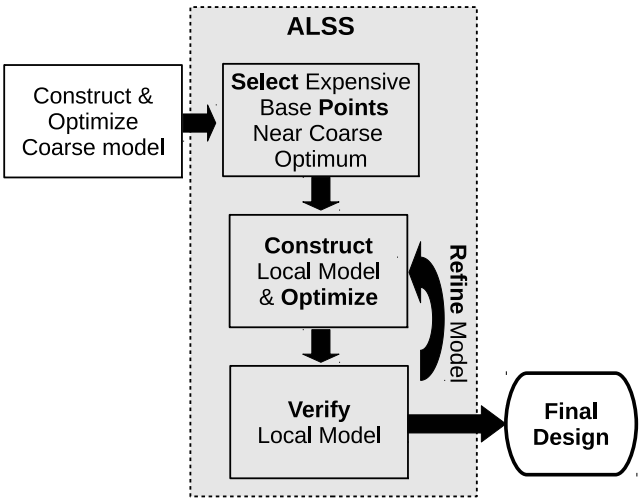

Fig. 12 Flow of ALSS-based iterative surrogate modelling technique used at the physical-layer optimization.

The surrogate model that is used for the local optimization spans the layout design parameters that are listed in Table 1. The following multidimensional regression approaches have been considered for this work: a table-lookup model, multivariate adaptive regression splines (MARS) [24], least-squares support vector machines (SVM) [25] and a deterministic symbolic regression technique, fast function extraction (FFX) [26]. Experiments showed that the table-lookup model captures the problem with sufficient accuracy and minimal model building effort.

After each optimization of the surrogate model, the model is iteratively updated with new training points for locally enhancing the accuracy. The selection of expensive training points is of importance, as they define the quality of the model, hence the quality of the optima. The sample selection algorithm developed in [10] is deployed here to ensure good design space exploration and good robustness of the surrogate model by finding a point $\mathbf{x}^*$ that maximizes the following distance function:

$$D_{tot}(\mathbf{x}^*) = D_x(\mathbf{x}^*) \cdot [1 + D_y(\mathbf{x}^*)]^{\alpha} \cdot \left[1 + D_{\mathrm{var}(\hat{y})}(\mathbf{x}^*)\right]^{\beta} \quad (12)$$

Here, $D_x(.)$ accounts for the exploration of the design space $\mathbf{x}$, $D_y(.)$ biases the samples to regions where strong nonlinearities occur in the data and $D_{\mathrm{var}(\hat{y})}(.)$ predicts the regions where the surrogate model $\hat{y}(\mathbf{x})$ is the least robust by means of bootstrapping [27]. α and β skew the weight of the distance function towards design space exploration ($\alpha = \beta = 0$) or towards accuracy of the surrogate model ($\alpha = \beta = 1$), see [10]. Each distance function component is implemented as follows:

$$\begin{cases} D_x(\mathbf{x}^*) = \min \parallel \mathbf{x}^* - \mathbf{x_L} \parallel_2 . \\ D_y(\mathbf{x}^*) = \parallel \dfrac{y_n - \hat{y}(\mathbf{x}^*)}{\max(y_L) - \min(y_L)} \parallel_2 . \\ D_{\mathrm{var}(\hat{y})}(\mathbf{x}^*) = \dfrac{\sigma^2(\hat{\mathbf{y}}_\mathbf{m}(\mathbf{x}^*))}{\sigma^2\left[\mu_{1/2}(\hat{\mathbf{y}}_\mathbf{m}(\mathbf{x}^*))\right]} \end{cases} \quad (13)$$

where $\mathbf{x_L}$ is a set of L base points and y_L are the corresponding EM simulation results. The degree of nonlinearity in the performance space is measured by the distance between the model output $\hat{y}(\mathbf{x}^*)$ and its nearest neighbour $y_n = y(\mathbf{x_n}) \in y_L$. The sensitivity of the model towards the data set is measured by building a series of models with slight variations on the training data, known as bootstrapping. The sensitivity of the model to the training data is then computed as the variance of these bootstrapped models. The model variance is further normalized to the variance of the median of each bootstrapped model [10], [27]. The surrogate model can now be updated with the point corresponding to the maximum value of the distance function (12).

5 Simulation results

An inductive DC-DC boost converter (1.2 V to 2.4 V) is designed in a 0.13 μm CMOS technology using a tapered inductor.

The optimization framework is used to optimize a large set of initial candidates towards the most optimal Pareto front in the end. Throughout this optimization, the framework moves along the different design views. Firstly, initial samples are generated for the high-level DAE model. The resulting Pareto front is shown in Fig. 13 as a dotted line. The optimal DAE results that were found are then used in SPICE simulations. The resulting Pareto front is depicted in Fig. 13 as a dashed line. It was mentioned in section 2.2 that the accuracy of the SPICE and DAE simulations is within a 3% accuracy range. This can now be confirmed by the simulation results in Fig. 13.

Table 2 Comparison of simulation results for an inductive DC-DC converter design using a regular, full and tapered inductor.

	Regular inductor (1 layer)	Full inductor (8 layers)	Tapered inductor
P_{out} at max efficiency	25.4 mW	25.7 mW	25.6 mW
P_{in} at max efficiency	43.3 mW	44.9 mW	39.7 mW
Max efficiency (with temperature effect)	**58.7** % (58 %)	**57.3** % (56.7 %)	**64.5** % (64 %)
$P_{out,max}$ (with temperature effect)	47 mW @$\eta = 52$ % (35.3 mW @ 49 %)	59 mW @$\eta = 54$ % (44.2 mW @ 52 %)	63 mW @$\eta = 54$ % (46.6 mW @ 52 %)
Inductor inductance	49.74 nH (1 layer)	49.62 nH (full)	49.57 nH (tapered)
Inductor area	2.29 mm^2	2.29 mm^2	2.29 mm^2
Inductor series resistance	5.05 Ω	1.44 Ω	3.46 Ω
Switching frequency	76.8 MHz	76.8 MHz	76.8 MHz
C_{out}	0.89 nF	0.89 nF	0.89 nF
$P_{loss,inductor}$ (% of $P_{loss,total}$)	9.2 mW (**51** %)	11.4 mW (**59.4** %)	6.3 mW (**44** %)
$P_{loss,total}$	18 mW (100 %)	19.2 mW (100 %)	14 mW (100 %)

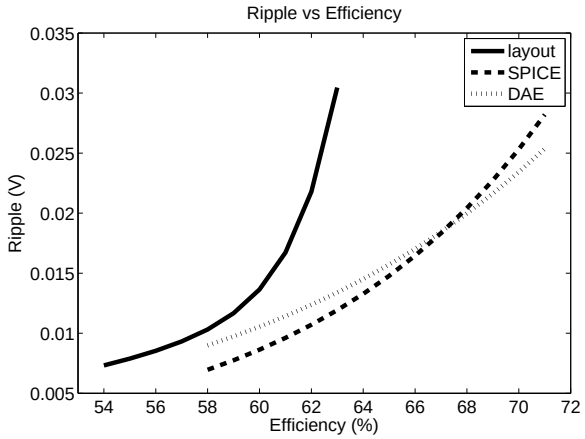

Fig. 13 Ripple vs. efficiency for DAE, SPICE and layout design views.

The final step in the optimization is the layout- and temperature-aware modeling. In this phase, the actual extracted parasitics of the inductor and the temperature effects are taken into account, combined with the already existing SPICE simulations for each resulting candidate DC-DC converter. This is the most accurate modeling in the optimization flow, yielding the Pareto front in Fig. 13, depicted as a continuous line. The efficiency of the resulting converters is lower compared to the DAE and SPICE results. This indicates that the parasitic substrate capacitance and thus the accurate modeling of the inductor are paramount for a realistic simulation. The major contribution of the inductor in the power losses was already discussed in [11].

Out of the layout-aware Pareto front, a final design point is then chosen. The properties of this design are summarized in Table 2. The simulation results are compared between the inductor using the tapered topology, an inductor with a regular topology, using only a thick top-metal layer and another regular inductor using eight metal layers. An inductor with 8 tapered metal layers and a resulting inductance of 49.57 nH is created with an area of 2.29 mm^2. As can be seen in Table 2, only a small difference in the inductance of the regular inductors exists. However, the efficiency of the converter using the tapered inductor is increased with 7 %, giving a total efficiency of 64.5 % instead of 57.3 % compared to a converter with a *full* inductor.

The temperature effects are considered as well. These have an influence on the maximum output power and must be taken into account. The tapering reduces the total power loss with as much as 27 %, going from 19.2 mW to 14 mW. This implicitly confirms the lower substrate capacitance in the tapered inductor. Also, the maximum output power has increased with 34 % from 47 mW to 63 mW (from 35.3 mW to 46.6 mW with temperature effects), compared to the regular inductor with one metal layer. These maximum output powers can be determined from Fig. 3. This figure presents the simulated results with and without temperature effects for the chosen final design point. The contribution of the inductor to the total power loss in the converter has dropped from 59 % to 44 %.

6 Conclusion

This paper has proposed a framework for the efficient optimization of fully-integrated inductive DC-DC converters, focusing on the losses in the on-chip inductor as well as on the accurate layout-based modeling of temperature effects. A tapered inductor topology has been introduced. The methodology has been demonstrated for the design of a fully-integrated DC-DC boost converter in a 0.13 μm CMOS technology. The power loss in the circuit is reduced with 27 % which results in a 7 % efficiency improvement, compared to a fully-integrated DC-DC boost converter with a regular inductor topology.

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